

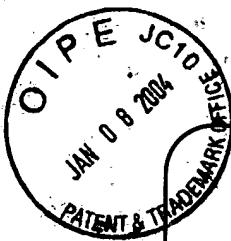
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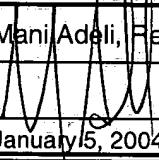
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		Application Number	10/066,456
		Filing Date	1/31/02
		First Named Inventor	Steven Teig, et al.
		Group Art Unit	2825
		Examiner Name	B. Tat
Total Number of Pages in This Submission		Attorney Docket Number	SPLX.P0099

Enclosures (Check all that apply)

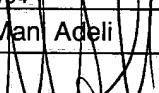
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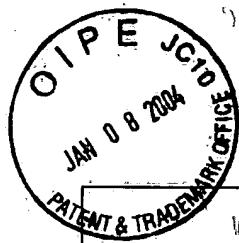
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PATENT
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Mani Adeli

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Steven Teig, et al.

Serial No.: 10/066,456

Filing Date: 1/31/02

For: METHOD AND APPARATUS FOR
PERFORMING TECHNOLOGY
MAPPING

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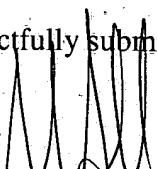
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Dated: January 5, 2004

Respectfully submitted,

By:


Mani Adeli
Registration No. 39,585

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P.O. Box 51860
Palo Alto, CA 94303-0728

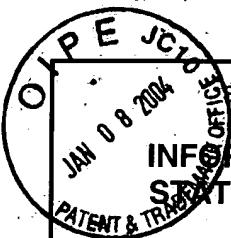
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(use as many sheets as necessary)

Sheet	1	of	2	Attorney Docket Number	SPLX.P0099
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U.S. PATENT DOCUMENTS

Examiner Initials	Cite No. ¹	U.S. Patent Document Number	Kind Code ² (if known)	Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	5,311,442		05-10-1994	Fukushima	
	2.	5,519,630		05-21-1996	Nishiyama et al.	
	3.	5,521,835		05-28-1996	Trimberger	
	4.	5,537,341		07-16-1996	Rose et al.	
	5.	5,610,829		03-11-1997	Trimberger	
	6.	5,696,974		12-09-1997	Agrawal et al.	
	7.	5,752,000		05-12-1998	McGeer et al.	
	8.	5,574,441		05-19-1998	Tokunoh et al.	
	9.	5,787,010		07-28-1998	Schaefer et al.	
	10.	6,023,566		02-08-2000	Belkhale et al.	
	11.	6,035,107		03-07-2000	Kuehlmann et al.	
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	13.	6,102,964		08-15-2000	Tse et al.	
	14.	6,301,696		11-09-2001	Lien et al.	
	15.	6,334,205	B1	12-25-2001	Iyer et al.	
	16.	6,336,208		01-01-2002	Mohan et al	
	17.	6,470478	B1	10-22-2002	Bargh et al.	
	18.	6,473,884		10-29-2002	Ganai et al	
	19.	6,496,972	B1	12-17-2002	Segal	
	20.	6,523,156	B2	02-18-2003	Cirit	
	21.	6,574,779	B2	06-03-2003	Allen et al.	

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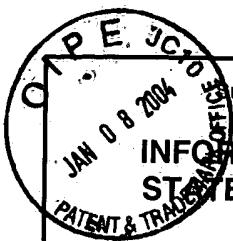
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				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2825
				Examiner Name	B. Tat
Sheet	2	of	2	Attorney Docket Number	SPLX.P0099

NON-PATENT LITERATURE DOCUMENTS			
Examiner* Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
	22.	Crastes, M. et al., A technology Mapping Method Based on Perfect and Semi-Perfect Matchings, Design Automation Conference, 1991, 28 th ACM/IEEE, June 17-21, 1991, pp. 93-98.	
	23.	Devadas, S. et al., Synthesis and Optimization for Robustly Delay-fault Testable Combinational Logic Circuits, Design Automation Conference, 1990, 27 th ACM/IEEE, June 24-28, 1990, pp.221-227.	
	24.	Yi, J. H. et al., Technology Mapping for Storage Elements Based on BDD matching, Proceedings of the 40 th Midwest Symposium on Circuits and Systems, pp. 1099-1102, vol.2, August 1997.	

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